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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,090	10/21/2003	Thomas J. Retelny JR.	NORTE-499A	4845
7663	7590	03/15/2005	EXAMINER	
STETINA BRUNDA GARRED & BRUCKER 75 ENTERPRISE, SUITE 250 ALISO VIEJO, CA 92656			CHOE, HENRY	
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 03/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

W-17

<b>Office Action Summary</b>	<b>Application No.</b> 10/690,090	<b>Applicant(s)</b> RETELNY, THOMAS J.	
	<b>Examiner</b> Henry K. Choe	<b>Art Unit</b> 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 February 2005.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 and 9-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5-8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Election*

Applicant provisionally elected the species IV without traverse. Applicant also designated that the claims 5-8 read on species IV. Examiner agrees with this statement. Therefore, it is concluded that the claims 1-4 and 9-20 are considered non-elected claims.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shih (Fig. 2).

Regarding claims 5 and 8, Shih (Fig. 2) discloses an amplifier circuit comprising an active bias circuit (Q1, Q2) which includes first (Q1) and second (Q2) FETs and each (Q1 or Q2) FET having a channel (a connection between Vref to source of Q1 or a connection between the Vabc to resistor R2) connected to a gate of the other FET (the connection between Vref to source of Q1 is connected to the gate of FET Q2 and the connection between the Vabc to resistor R2 is connected to the gate of FET Q1) to regulate an amount of current flowing through the channels (a connection between Vref to source of Q1 and a connection between Vabc to resistor R2) of the first (Q1) and second (Q2) FETs in the same manner as the claimed invention, and the wherein the

current flowing through the second FET (Q2) sets the biasing voltage at the gate (gate of Q1) of the first FET (Q1). As described above, Shih (Fig. 2) discloses all the limitations in the claim except for that the active bias circuit being formed on the wafer. It is well known to those of ordinary skill in the art to integrate a semiconductor device in order to form a small sized integrated Circuit. Therefore, it would have been obvious to have integrated the circuit of the reference (Shih) because such a modification would have advantageously produced a small size integrated circuit amplifier. As a consequence of forming the integrated circuit with a particular material, such as the wafer, which is well known in the art as obvious design choice.

Regarding claim 6, the first (Q1) and second (Q2) FETs have n-type channels.

Regarding claim 7, an output (drain terminal of PA) of the electrical circuit (Fig. 2) is connected to the channels (a connection between Vref to source of Q1 and a connection between Vabc to resistor R2) of the first (Q1) and second (Q2) FETs.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

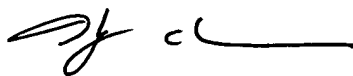
Patent numbers (5,625,313; 6,861,908; 6,326,849) are the amplifier circuits with the bias circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

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A handwritten signature in black ink, appearing to read 'H. Choe', with a long horizontal stroke extending to the right.

**HENRY CHOE**  
**PRIMARY EXAMINER**

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